Amendments to the Claims

1.-28. (canceled)

Please add the following claims.

29. (new) A method, comprising:

receiving, at a bridge device, a read request from an expansion device;

issuing a read request from the bridge device to a portion of a system memory predetermined to have descriptor addresses associated with the read request;

receiving descriptor blocks including descriptor data at the bridge device, wherein the descriptor data includes a transmit size, a location of the transmit data, and an address of the data to be transmitted;

storing the descriptor data in a memory on the bridge;

transmitting the descriptor blocks to the expansion device;

receiving a read request for data associated with the descriptor blocks;

searching the memory for the descriptor addresses; and

if the descriptor addresses are located in the memory on the bridge, fetching the data requested and prefetching any remaining data to match the transmit size.

30. (new) The method of claim 29, wherein storing the descriptor data comprises storing the descriptor data in a hash table.

31. (new) The method of claim 30, wherein searching the memory further comprises searching the hash table using a read request address as a key.

32. (new) The method of claim 29, the method comprising prefetching the data by cacheline, if the descriptor addresses are not locating in the memory.

33. (new) The method of claim 29, wherein storing the descriptor data comprises:

determining that the memory is full;

discarding an oldest descriptor in the memory; and

storing the descriptor in the memory.

34. (new) A processor having software that causes the processor to:

receive, at a bridge device, a read request from an expansion device;

issue a read request from the bridge device to a portion of a system memory predetermined to have descriptor addresses associated with the read request;

receive descriptor blocks including descriptor data at the bridge device, wherein the descriptor data includes a transmit size, a location of the transmit data, and an address of the data to be transmitted;

store the descriptor data in a memory on the bridge;

transmit the descriptor blocks to the expansion device;

receive a read request for data associated with the descriptor blocks;

search the memory for the descriptor addresses; and

if the descriptor addresses are located in the memory on the bridge, fetch the data requested and prefetching any remaining data to match the transmit size.

35. (new) The processor of claim 34, the software causing the processor to store the descriptor data comprises storing the descriptor data in a hash table.

36. (new) The processor of claim 34, the software causing the processor to search the memory further comprises searching the hash table using a read request address as a key.

37. (new) The processor of claim 34, the software causing the processor to prefetch the data by cacheline, if the descriptor addresses are not locating in the memory.

38. (new) A bridge device, comprising:

a first port to allow the device to communicate with other devices on an expansion bus;

a second port to allow the device to communicate with devices on a second bus;

a memory to store data; and

a processing element to:

receive, at a bridge device, a read request from an expansion device;

issue a read request from the bridge device to a portion of a system memory predetermined to have descriptor addresses associated with the read request;

receive descriptor blocks including descriptor data at the bridge device, wherein the descriptor data includes a transmit size, a location of the transmit data, and an address of the data to be transmitted;

store the descriptor data in a memory on the bridge;

transmit the descriptor blocks to the expansion device;

receive a read request for data associated with the descriptor blocks;

search the memory for the descriptor addresses; and

if the descriptor addresses are located in the memory on the bridge, fetch the data requested and prefetching any remaining data to match the transmit size.

39. (new) The device of claim 38, the processing element to store the descriptor data comprises storing the descriptor data in a hash table.

40. (new) The device of claim 38, the processing element to search the memory further comprises searching the hash table using a read request address as a key.

41. (new) The device of claim 38, the processing element to prefetch the data by cacheline, if the descriptor addresses are not locating in the memory.

42. (new) A bridge device, comprising:

a means for allowing the device to communicate with other devices on an expansion bus;

a means for allowing the device to communicate with devices on a second bus;

a means for storing data; and

a means for:

receiving, at a bridge device, a read request from an expansion device;

issuing a read request from the bridge device to a portion of a system memory predetermined to have descriptor addresses associated with the read request;

receiving descriptor blocks including descriptor data at the bridge device, wherein the descriptor data includes a transmit size, a location of the transmit data, and an address of the data to be transmitted;

storing the descriptor data in a memory on the bridge;

transmitting the descriptor blocks to the expansion device;

receiving a read request for data associated with the descriptor blocks;

searching the memory for the descriptor addresses; and

if the descriptor addresses are located in the memory on the bridge, fetching the data requested and prefetching any remaining data to match the transmit size.